one or more processors/computers, hardware (one or more apparatuses), firmware (one or more apparatuses), software (one or more modules), or combinations thereof. For a firmware or software, implementation can be through modules (e.g., procedures, functions, and so on) that perform the functions described herein. Software codes may be stored in any suitable, processor/computer-readable data storage medium(s) or memory unit(s) or article(s) of manufacture and executed by one or more processors/computers.

[0070] The apparatus may generally include a processor, controller, control unit, micro-controller, or the like connected to a memory and to various interfaces of the apparatus. Generally the processor is a central processing unit, but the processor may be an additional operation processor. Each or some or one of the units and/or algorithms described herein may be configured as a computer or a processor, or a microprocessor, such as a single-chip computer element, or as a chipset, including at least a memory for providing storage area used for arithmetic operation and an operation processor for executing the arithmetic operation. Each or some or one of the units and/or algorithms described above may comprise one or more computer processors, application-specific integrated circuits (ASIC), digital signal processors (DSP), digital signal processing devices (DSPD), programmable logic devices (PLD), field-programmable gate arrays (FPGA), and/or other hardware components that have been programmed in such a way to carry out one or more functions of one or more embodiments/implementations/examples. In other words, each or some or one of the units and/or the algorithms described above may be an element that comprises one or more arithmetic logic units, a number of special registers and control circuits.

[0071] Further, the apparatus may generally include volatile and/or non-volatile memory, for example EEPROM, ROM, PROM, RAM, DRAM, SRAM, double floating-gate field effect transistor, firmware, programmable logic, etc. and typically store content, data, or the like. The memory or memories may be of any type (different from each other), have any possible storage structure and, if required, being managed by any database management system. The memory may also store computer program code such as software applications (for example, for one or more of the units/algorithms) or operating systems, information, data, content, or the like for the processor to perform steps associated with operation of the apparatus in accordance with examples/embodiments. The memory, or part of it, may be, for example, random access memory, a hard drive, or other fixed data memory or storage device implemented within the processor/apparatus or external to the processor/apparatus in which case it can be communicatively coupled to the processor/network node via various means as is known in the art. An example of an external memory includes a removable memory detachably connected to the apparatus.

[0072] The apparatus may generally comprise different interface units, such as one or more receiving units for receiving user data, control information, requests and responses, for example, and one or more sending units for sending user data, control information, responses and requests, for example. The receiving unit and the transmitting unit each provides an interface in an apparatus, the interface including a transmitter and/or a receiver or any other means for receiving and/or transmitting information, and performing necessary functions so that the control information, etc. can be received and/or sent. The receiving and sending units may comprise a set of antennas, the number of which is not limited to any particular number.

[0073] Further, the apparatus may comprise other units, such as one or more user interfaces for receiving user inputs and/or outputting information to the user.

[0074] It will be obvious to a person skilled in the art that, as technology advances, the inventive concept can be implemented in various ways. The invention and its embodiments are not limited to the examples described above but may vary within the scope of the claims.

[0075] It will be obvious to a person skilled in the art that, as technology advances, the inventive concept can be implemented in various ways. The invention and its embodiments are not limited to the examples described above but may vary within the scope of the claims.

1. A method comprising:

receiving as input a required maximum capacity for sounding or discovery and a maximum tolerated latency for a service group comprising one or more apparatuses being configured to use half-duplex wireless device-to-device communication;

selecting a pattern group from a set of pattern groups based on the received input; and

configuring physical resources for the half-duplex wireless device-to-device communication to the service group to have, for sounding or discovery within the service group, one or more patterns in the selected pattern group, a pattern defining for the physical resources a number of serial resources, a number of parallel resources and a number of transmission phases.

2. A method as claimed in claim **1**:

wherein selecting a pattern group is based on the total number of resources; and

wherein each pattern group is characterized by at least one of the following properties:

the number of patterns, the number of parallel resources, the number of serial resources, and the number of transmission phases.

3. A method as claimed in claim **1**, wherein the selecting a pattern group comprises:

calculating a number of patterns in a pattern group for the set of pattern groups, the set starting from a pattern group comprising one serial resource and having one transmission phase and ending to a pattern group comprising an amount of serial resources corresponding to the maximum tolerated latency and having at most as many transmission phases as there are parallel resources;

calculating a number of parallel resources required in a pattern group for the pattern groups;

calculating total number of resources in a pattern group for the pattern groups; and

selecting amongst the pattern groups one pattern group whose number of patterns provide the required maximum capacity for sounding or discovery with a minimum total number of resources.

4. A method as claimed in claim **3**, further comprising:

determining the number of parallel resources, the number of serial resources, the number of patterns and the number of transmission phases in said selected one pattern group using calculation results;

creating patterns for sounding or discovery of the service group using the determined number of parallel resources, the determined number of serial resources,